Physical Verification Engineer (m/f)

Job No. 001850

Position Type:

Research & Development

Working Time:

Regular Fulltime

Job description / tasks and responsibilities:

- Maintainance of Physical Verification rule-files for CMOS, HV CMOS, EEPROM and Opto processes for analog/mixed signal, high voltage, RF and 3D-integrated sensor applications
- Technical support for Mentor CALIBRE SVRF and PERC, Cadence Assura and PVS related to DRC, LVS, ERC, PEX, ANT and DFM rule files
- Support for Physical Verification related to external and internal PDKs

Education/Experience:

- Master's or Bachelor degree in physics or electrical engineering
- Professional experience with Physical Layout Verification (e.g. Mentor CALIBRE SVRF, PERC, Cadence Assura and PVS, Synopsis)
- Basic knowledge in Linux shell script languages (e.g. tcsh, Tcl, Perl)
- Basic know-how in semiconductor physics and processing
- Basic knowledge in EDA tools
- Knowledge in mask data preparation is advantageous

Place of Employment:

Premstaetten / Austria / Europe

Collective salary and wage agreement:

We offer competitive salaries and additional benefits

based on your performance, experience and qualification.

The employment is in accordance with the collective salary and wage agreement for employees of the electrical and electronics industry, employment group F (http://www.feei.at/kollektivvertraege/kv_tabelle/).

We offer a higher compensation depending on your expertise and skills.

Online Application

URL: www.ams.com/eng/Join-Our-Team/Open-Positions/Physical-Verification-Engineer-m-f